

Claims

- [c1] A method for fabricating an integrated structure including a semiconductor device and connector structures for connecting the semiconductor device to a motherboard, the method comprising the steps of:
- forming a first layer on a plate transparent to ablating radiation, the first layer having a first set of conductors disposed therein, the first set of conductors connecting to bonding pads, the bonding pads being spaced with a first spacing distance in accordance with a required spacing of connections to the motherboard;
 - forming a second layer on the semiconductor device, the second layer having a second set of conductors disposed therein connecting to the semiconductor device;
 - forming studs on one of the first layer and the second layer and a third layer on the other of the first layer and the second layer, the studs being spaced with a second spacing distance less than the first spacing distance;
 - forming vias in the third layer, the vias being spaced in accordance with the second spacing distance;
 - aligning the studs to the vias;
 - attaching the semiconductor device to the first layer, so that the first set of conductors and the second set of

conductors are connected through the studs; ablating an interface between the first layer and the plate using ablating radiation transmitted through the plate, thereby detaching the plate; and attaching the connector structures to the bonding pads.

- [c2] A method according to claim 1, further comprising the step of:
attaching a support structure to the first layer, so that the support structure surrounds the semiconductor device.
- [c3] A method according to claim 1, wherein the connector structures form one of a pin grid array (PGA), a ball grid array (BGA), a C4 array and a land grid array (LGA).
- [c4] A method according to claim 2, wherein said step of attaching the support structure is performed before said step of attaching the semiconductor device and before said ablating step.
- [c5] A method according to claim 2, wherein said step of attaching the support structure is performed after said step of attaching the semiconductor device and before said ablating step.
- [c6] A method according to claim 2, wherein the mother-board is characterized by a thermal coefficient of expansion

sion (TCE), and the support structure is provided with a TCE approximately that of the motherboard.

- [c7] A method according to claim 2, wherein the support structure has an area corresponding to an area occupied by the bonding pads.
- [c8] A method according to claim 2, further comprising the step of filling a gap between the semiconductor device and the surrounding support structure.
- [c9] A method according to claim 1, further comprising the step of exposing the bonding pads, before said step of attaching the connector structures.
- [c10] A method according to claim 1, wherein the studs are formed on the first layer, and the first layer is provided with an adhesive layer for bonding to the third layer.
- [c11] A method according to claim 1, wherein the second set of conductors is arranged in a plurality of metal layers, the number of said metal layers being less than a number of layers required for fanout to the bonding pads spaced with the first spacing distance.
- [c12] A method for fabricating an integrated structure including a semiconductor device and connector structures for connecting the semiconductor device to a motherboard,

the method comprising the steps of:

forming a first layer on a plate transparent to ablating radiation, the first layer having a first set of conductors disposed therein, the first set of conductors connecting to bonding pads, the bonding pads being spaced with a first spacing distance in accordance with a required spacing of connections to the motherboard;

forming a second layer on the semiconductor device, the second layer having a second set of conductors disposed therein connecting to the semiconductor device;

forming a plurality of C4 connectors on the second layer, the C4 connectors being spaced with a second spacing distance less than the first spacing distance;

aligning the C4 connectors to the first layer;

attaching the C4 connectors to the first layer, so that the first set of conductors and the second set of conductors are connected;

ablating an interface between the first layer and the plate using ablating radiation transmitted through the plate, thereby detaching the plate; and

attaching the connector structures to the bonding pads.

- [c13] A method according to claim 12, further comprising the step of:
- attaching a support structure to the first layer, so that the support structure surrounds the semiconductor de-

vice.

- [c14] A method according to claim 12, wherein the connector structures form one of a pin grid array (PGA), a ball grid array (BGA), a C4 array and a land grid array (LGA).
- [c15] A method according to claim 13, wherein said step of attaching the support structure is performed before said step of attaching the semiconductor device and before said ablating step.
- [c16] A method according to claim 13, wherein the motherboard is characterized by a thermal coefficient of expansion (TCE), and the support structure is provided with a TCE approximately that of the motherboard.
- [c17] A method according to claim 13, wherein the support structure has an area corresponding to an area occupied by the bonding pads.
- [c18] A method according to claim 13, further comprising the step of filling a gap between the semiconductor device and the support structure and a gap between the semiconductor device and the first layer surrounding the C4 connectors.
- [c19] A method according to claim 12, further comprising the step of exposing the bonding pads, before said step of

attaching the connector structures.

- [c20] A method according to claim 12, wherein the second set of conductors is arranged in a plurality of metal layers, the number of said metal layers being less than a number of layers required for fanout to the bonding pads spaced with the first spacing distance.
- [c21] An integrated structure including a semiconductor device and connector structures for connecting the semiconductor device to a motherboard, the integrated structure comprising:
 - a first layer having a first set of conductors disposed therein, the first layer having an upper surface and a lower surface, the first set of conductors connecting to bonding pads disposed on the lower surface, the bonding pads being spaced with respect to each other with a first spacing distance in accordance with a required spacing of connections to the motherboard;
 - the semiconductor device;
 - a second layer disposed on the semiconductor device and in contact therewith, the second layer having a second set of conductors disposed therein connecting to the semiconductor device, the second layer facing the first layer;
 - a plurality of connectors connecting the first set of conductors to the second set of conductors, said connectors

being one of (1) a set of stud/via connectors and (2) a set of C4 connectors, said connectors being spaced with respect to each other with a second spacing distance less than the first spacing distance;

a support structure attached to the upper surface of the first layer and surrounding the semiconductor device, a gap between said support structure and the semiconductor device being filled with a fill material; and connector structures connected to the bonding pads.

- [c22] An integrated structure according to claim 21, wherein the connector structures form one of a pin grid array (PGA), a ball grid array (BGA), a C4 array and a land grid array (LGA).
- [c23] An integrated structure according to claim 21, wherein the motherboard is characterized by a thermal coefficient of expansion (TCE), and the support structure is provided with a TCE approximately that of the motherboard.
- [c24] An integrated structure according to claim 21, wherein the support structure has an area corresponding to an area occupied by the bonding pads.
- [c25] An integrated structure according to claim 21, wherein said plurality of connectors are a set of C4 connectors,

and the fill material fills a gap between the semiconductor device and the first layer surrounding said C4 connectors.

- [c26] An integrated structure according to claim 21, wherein said plurality of connectors are a set of stud/via connectors, and said integrated structure further comprises a third layer interposed between the first layer and the second layer and having vias formed therein.